Engineering at Fermilab:

Microelectronics for Next-Generation Instrumentation

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PPD/FQI Quantum ASIC Group

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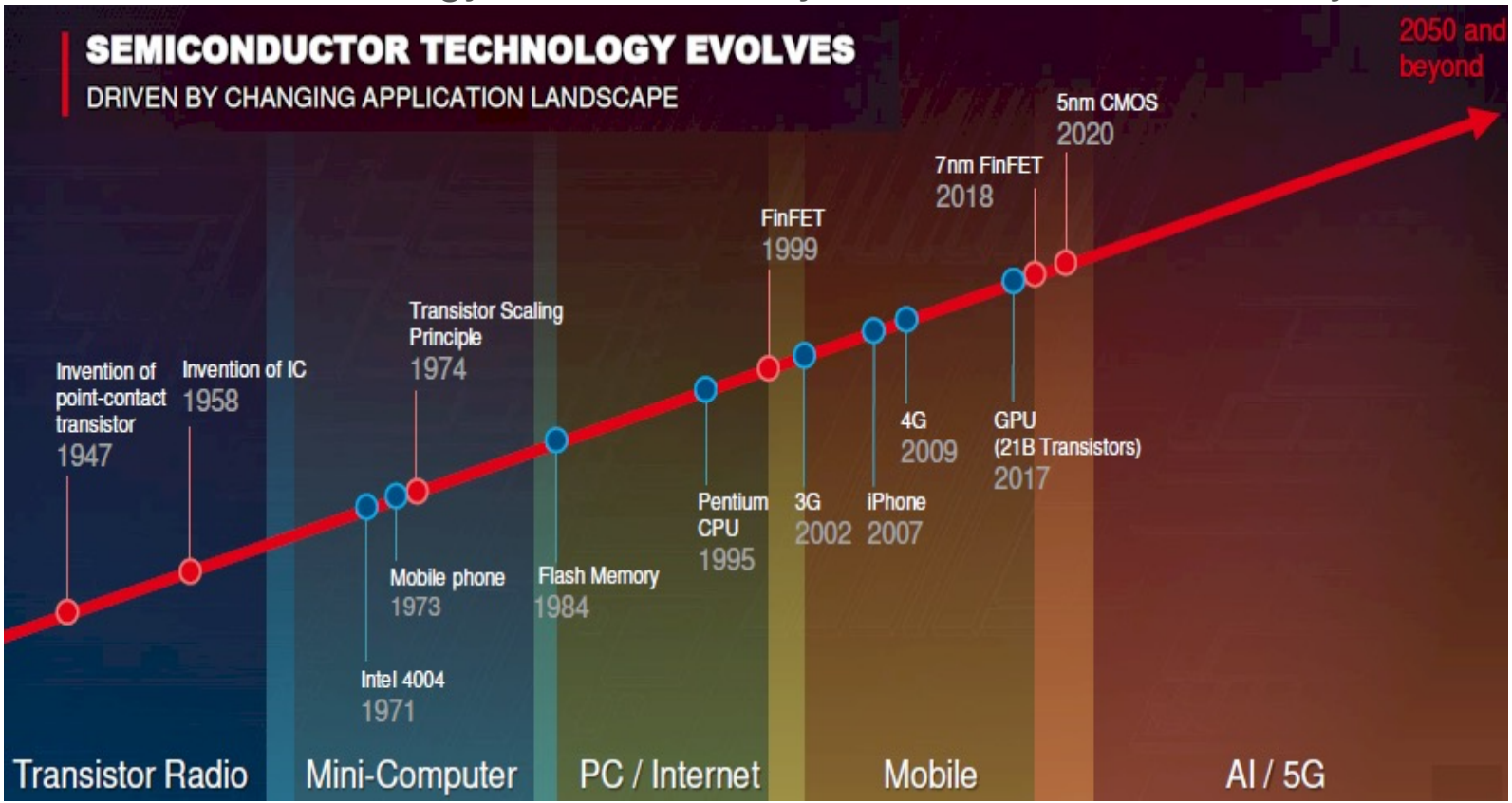
Microelectronics Growth

Moore's law: technology scales 2× every 18 months – sustained by transistor scaling.



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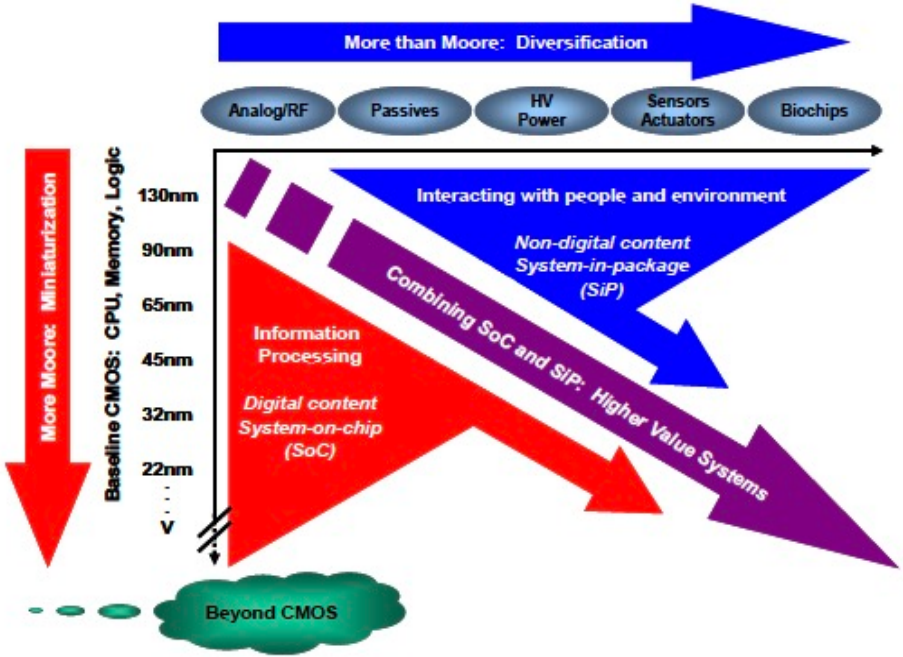
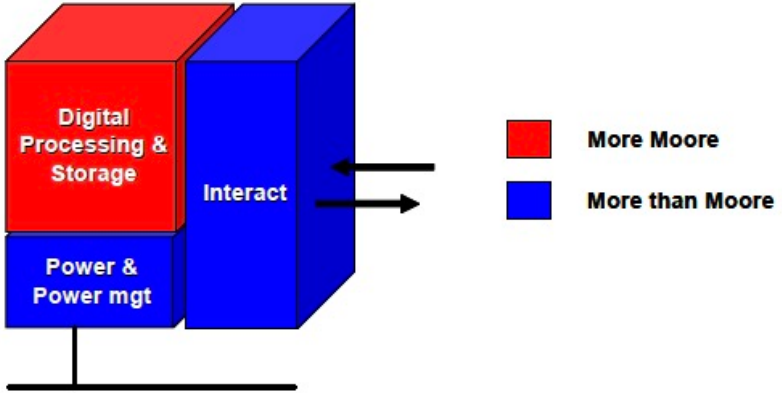
Diversified On-Chip Functionalities

- World is inherently analog or mandates an analog interface.
- Systems require various functions: analog/RF interface, analog-digital conversion, digital signal processing and storage, power management.
- Multi technology platforms





Source: ITRS

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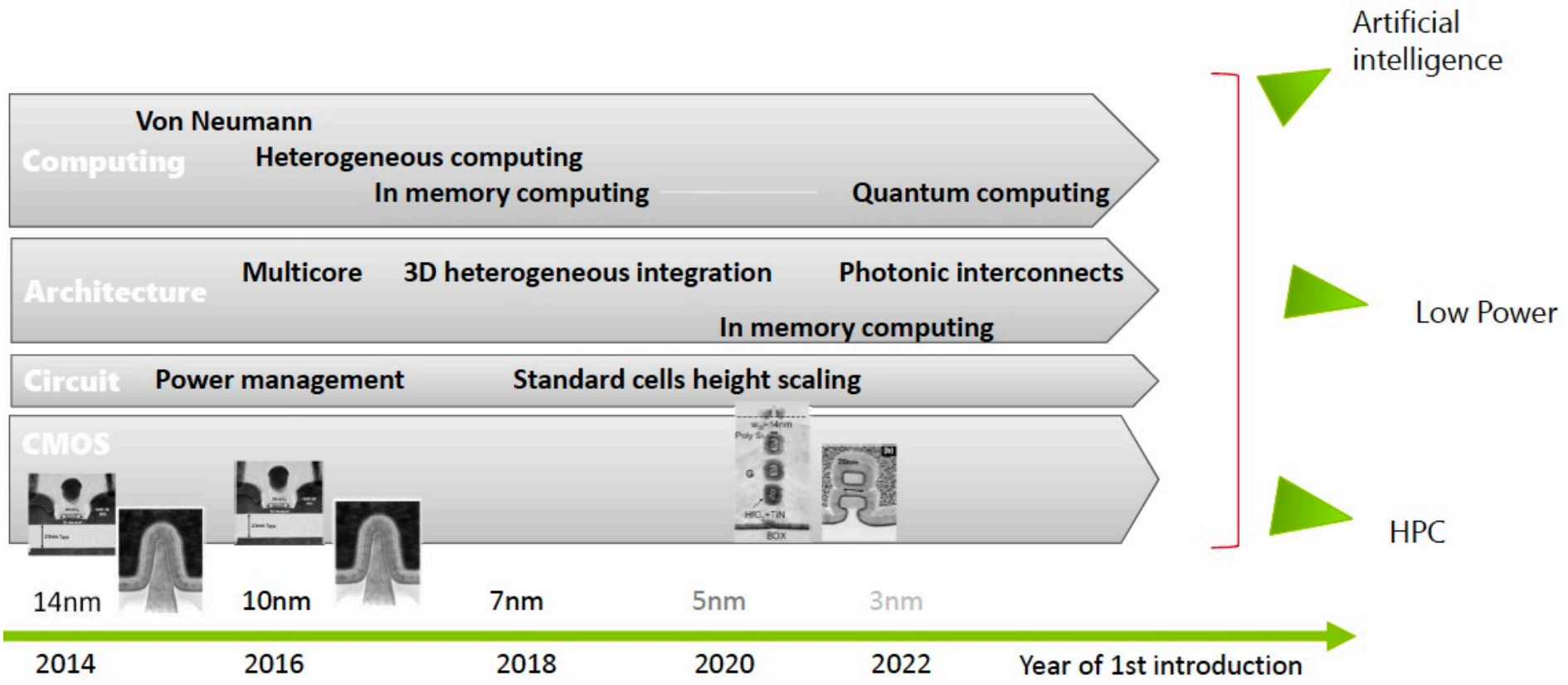
Why do we need more than Moore

Source: CEA- LETI



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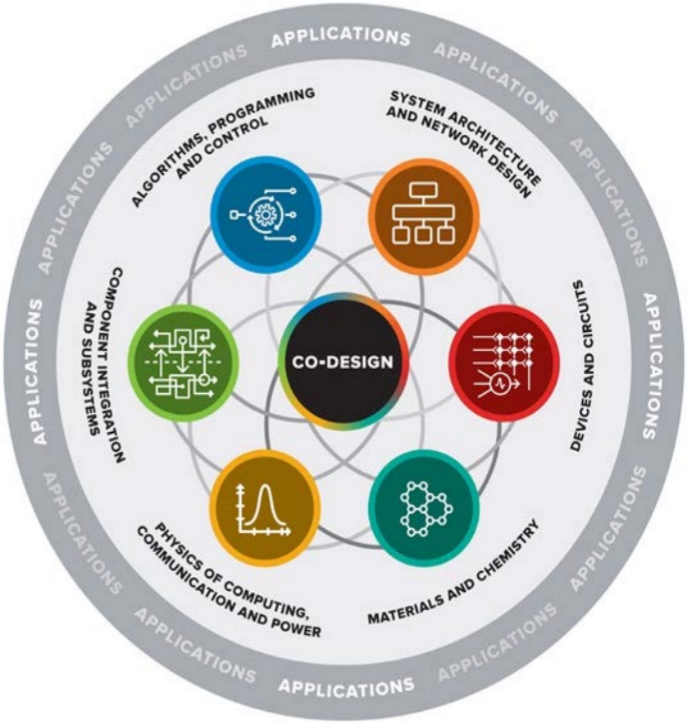
Microelectronics enabling next-generation instrumentation

- **Novel devices**
  - Skipper CCD-in-CMOS
- **Deep Cryogenic electronics**
  - Quantum Communication & Computing
- **Hybrid integration**
  - Electronic – Photonic Integration
  - 3D integration
- **Hardware – Software codesign to enable edge compute**
  - On-chip machine learning



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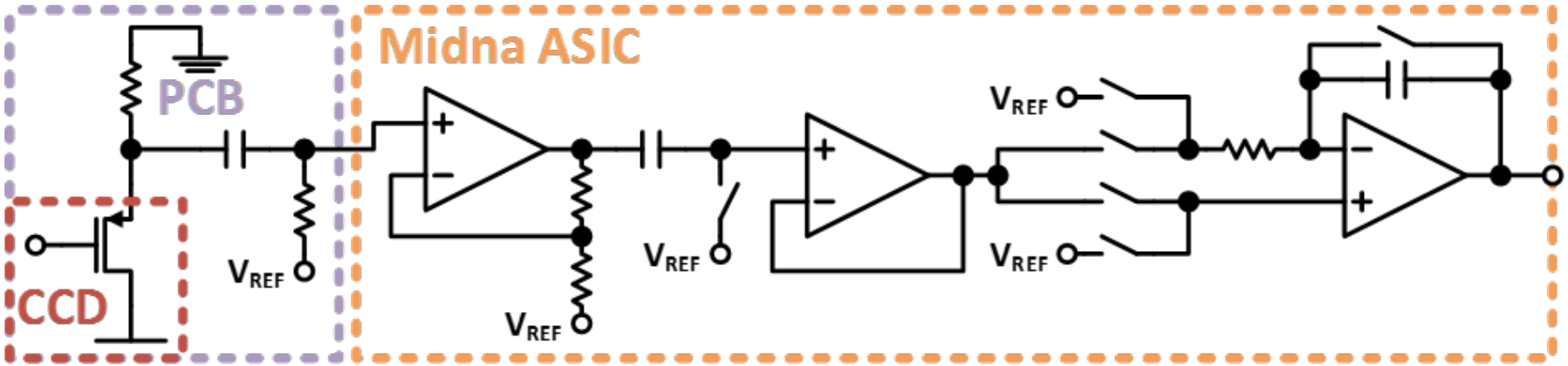
Novel Devices

Future CCD technologies

- **Fermilab has been pioneering Skipper CCD technologies – Averaging multiple samples for ultra-low noise performance (~ 1000 averages for << 1e- noise) – Juan Estrada**

- 1st Step – Enable parallel readout with low-cost multiple channels. Translate PCB design to Readout Integrated Circuit (ROIC) with lower noise performance (1/3rd CCD noise) and ~8 mW power per channel.
- 4” × 4” board to ~ 4 × 4 mm^2
- Cost reduction of ~100×

T. England, F. Alcalde Bessia, H. Sun, L. Stefana (SCD)



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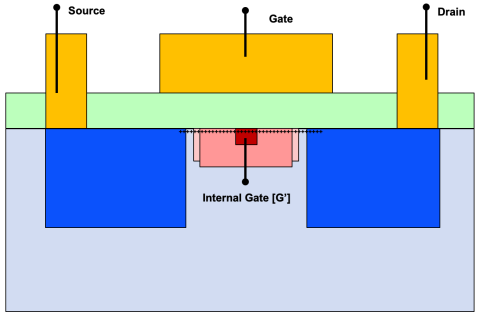
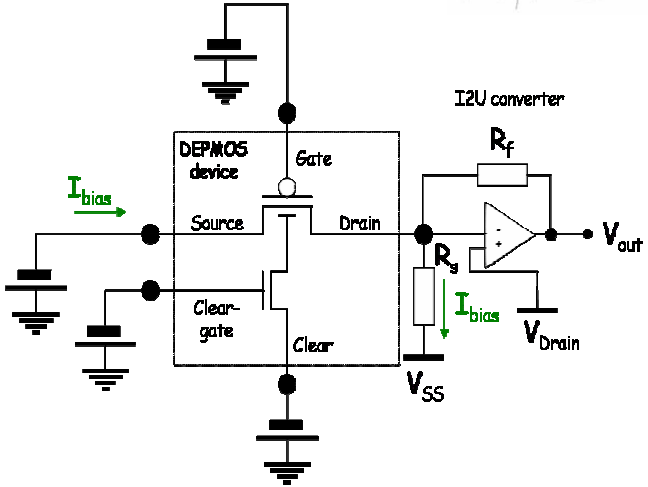
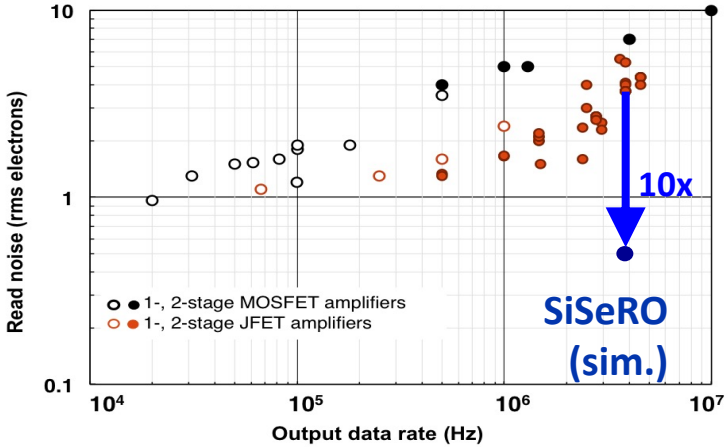
Future CCD technologies

M. SofoHaro (CNEA), K. Donovan (MIT LL)

- 2nd Method – Increase readout speed without increasing noise: SiSeRO (collaboration with MIT Lincoln Lab)
- 10 × speed improvement
- Additional advantages: readout is DC-coupled at low operating voltages which removes AC coupling capacitors and further increases system integration and reduces footprint)







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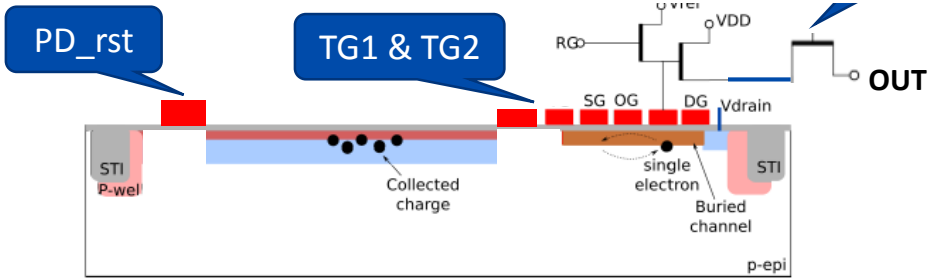
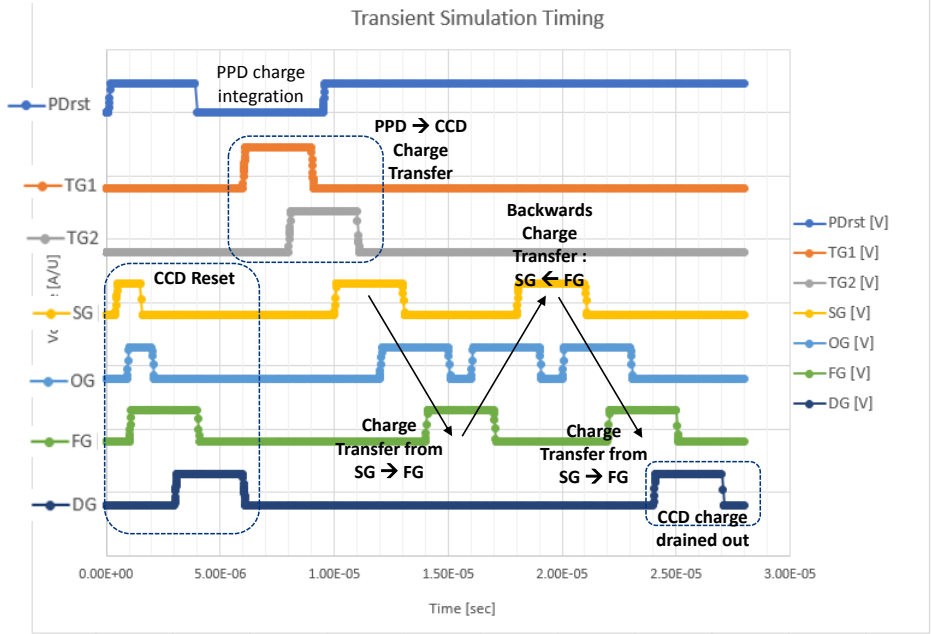
Future CCD technologies

M. SofoHaro (CNEA), A. Birman (Tower)

- 2-D approach: skipper-in-CMOS
- Utilize a commercial CMOS Image Sensor process for lower noise performance (collaboration with SLAC and Tower Semiconductor).
- Noise of a pinned photodiode: 0.7 e-.
- With 10 averages we plan to achieve noise of ~0.2 e-.
- Allows hybrid pixel sensor with fully-parallel per-pixel readout achieving the ultimate goal of 1 kfps readout over large areas (~6 cm^2) of ~2.5 Mpixels per chip.





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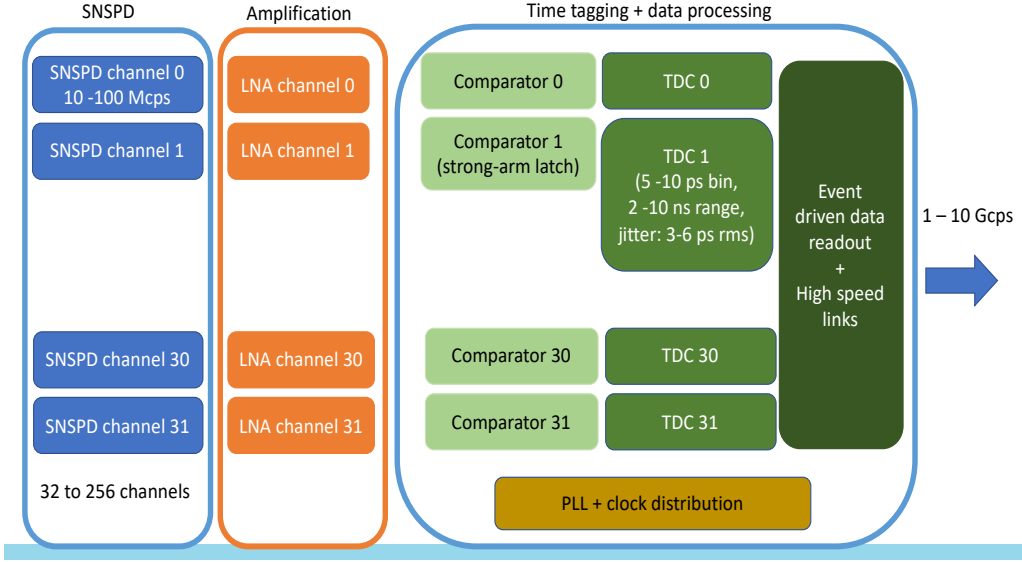
Deep Cryoelectronics for Quantum Computing

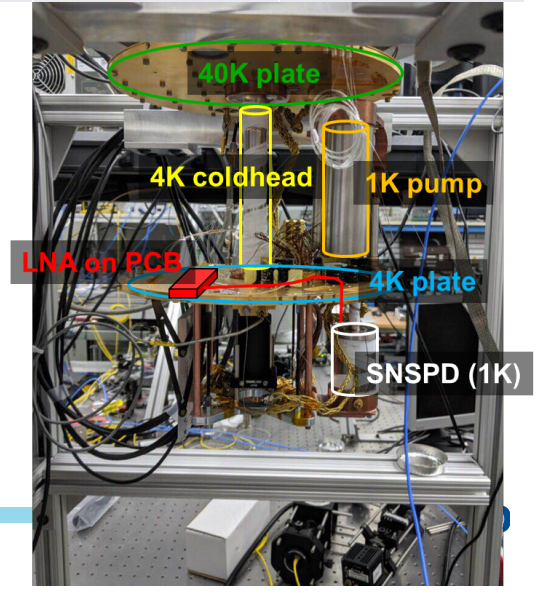
Quantum Communication: Superconducting Nanowire Single Photon Detectors (SNSPD)

- SNSPD best performance: operating at 1 - 4K.
- Time-correlated single photon counting from the deep UV to the mid-infrared.
- Extremely low dark counts and very high precision.
- QUANTUM INTERNET: high bandwidth communication.

1st Step – Low-noise amplification in collaboration with Georgia Tech and JPL.



Parameter	Goal by 2025	SOA 2019
Efficiency	>80% @ 10 μm	98% @ 1550 nm
Dark Counts	< 1e-6 cps / mm^2	< 1e-4 cps / mm^2
Energy Threshold	12.5 meV (100 μm)	0.125 eV (10 μm)
Timing Jitter	< 1 ps	2.7 ps
Active Area	100 cm^2	0.92 mm^2
Max Count Rate	100 Gcps	1.2 Gcps
Pixel Count	1.6e7 (4096x4096)	1024 (32x32)



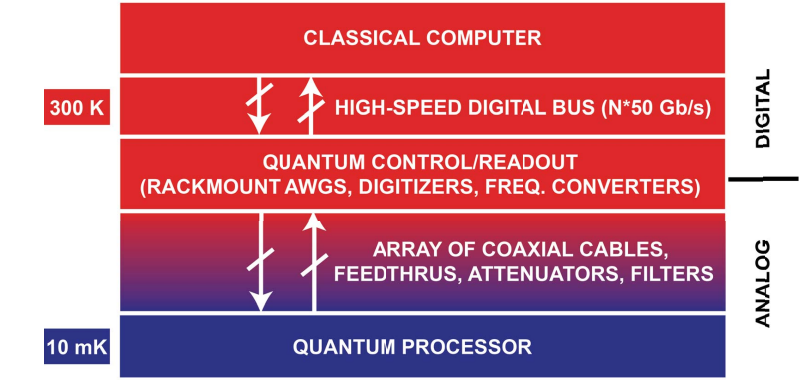
D. Braga

Beyond NISC era QC Utilizing Cryo-Electronics

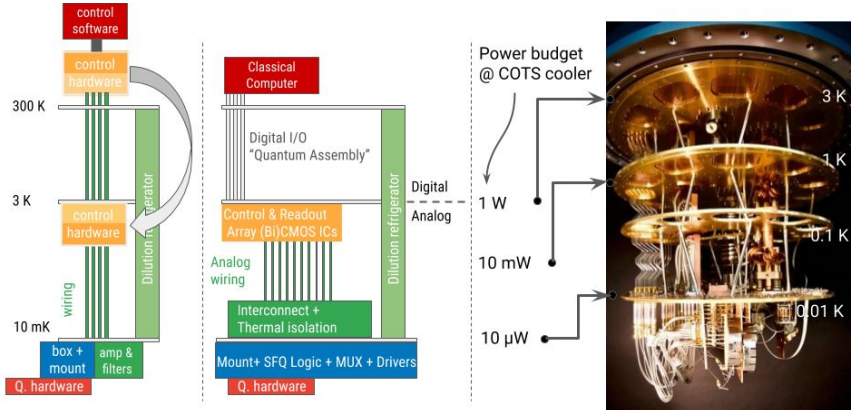
- Collaboration with industry: (Microsoft – High speed ADC)
- High-speed and high-resolution are often conflicting goals.
- Key transistor behavior: faster speed and low noise performance at cryogenic temperature.
- Why National Lab - cryogenic electronics for DUNE (full cycle from modelling to testing).
- Modelling is key (collaboration with EPFL/ TU Delft).

T. England, D. Braga

Architecture Suitable for 72 Qubit Computer



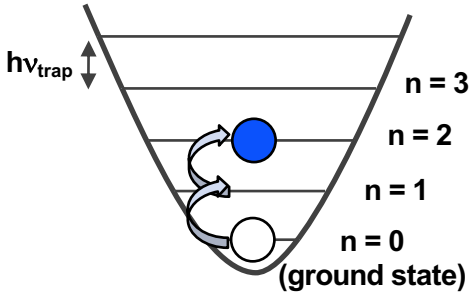
Scale by Integrating Control Electronics

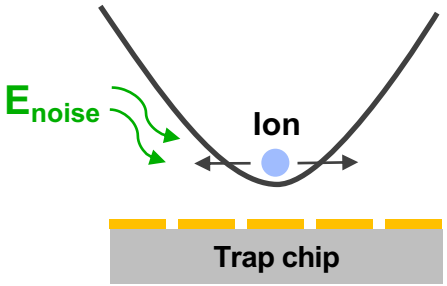


Google AI Quantum

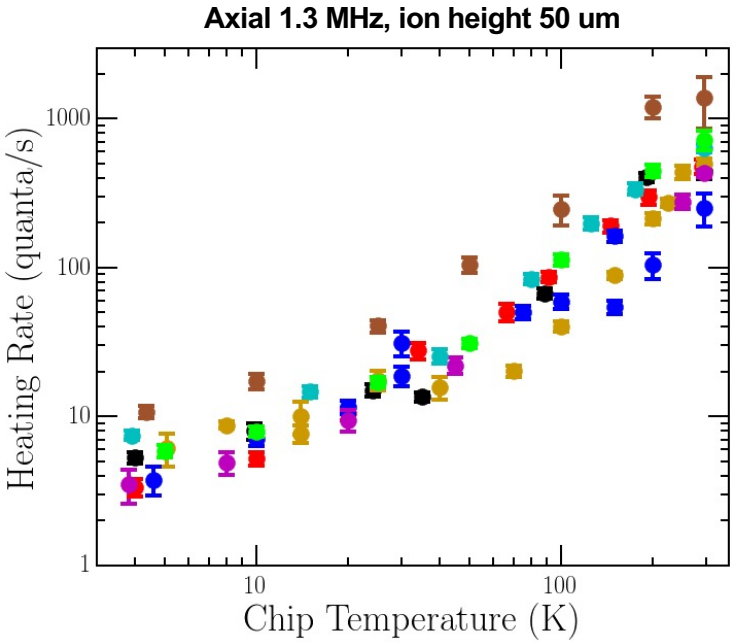
Benefits of Cryogenics for Trapped-Ion QIP

J. Chiaverini,
MIT LL





- **Greatly reduced electric-field noise**
  - **This noise is a limiting factor in error in trapped-ion 2QGs in small traps**
  - **Measured to be much larger than JN ("anomalous")**
  - **Source unknown**
  - **Empirically, 2 orders of magnitude lower at ~5K when compared to room temp.**
  - **This is true when technical noise is under control**



MIT-LL measurements

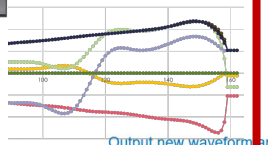
QIP: Quantum information processing
2QG: Two-qubit gate
JN: Johnson noise

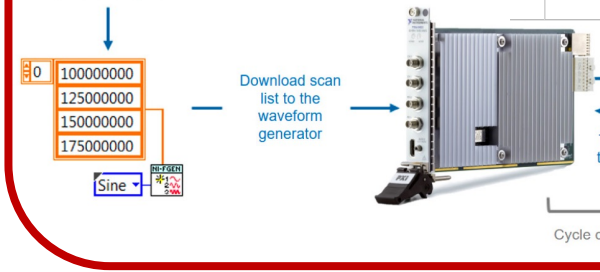
Cryo-Electronics Control for Ion-Traps (QSC - ORNL)

S. Li, F. Fahim (FNAL)
C. Seck, R. Pooser (ORNL)

with expensive and bulky room-operation electronics

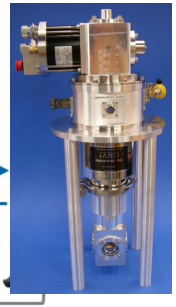
Commercial waveform generators
(need 12 modules of 8 channels each)





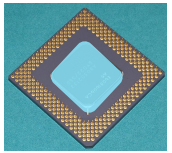
Sandia ion traps

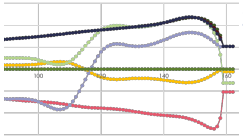
4 K cryocooler



with compact low-power cryogenic ASIC

Cryogenic ion trap controller ASIC (96 channels)





Sandia ion traps

All inside the 4 K cryocooler

- Low output noise: < 100 nV/sqrt(Hz) around a wide frequency range (0.5 - 5 MHz) and at low frequency.
- Low power: < 5 mW/DAC (limited by the cooling power of the cryostat) while driving a wide rage of load capacitance (70 – 1800 pF) of +/- 10 V full scale at 10 MHz waveform updating rate.
- High resolution: 14-16 bit for precise control and not disturbing RF electrodes.
- Memory: 100 electrodes * 14 bit * 5000 points ~ 2.5 MB

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Hybrid Integration

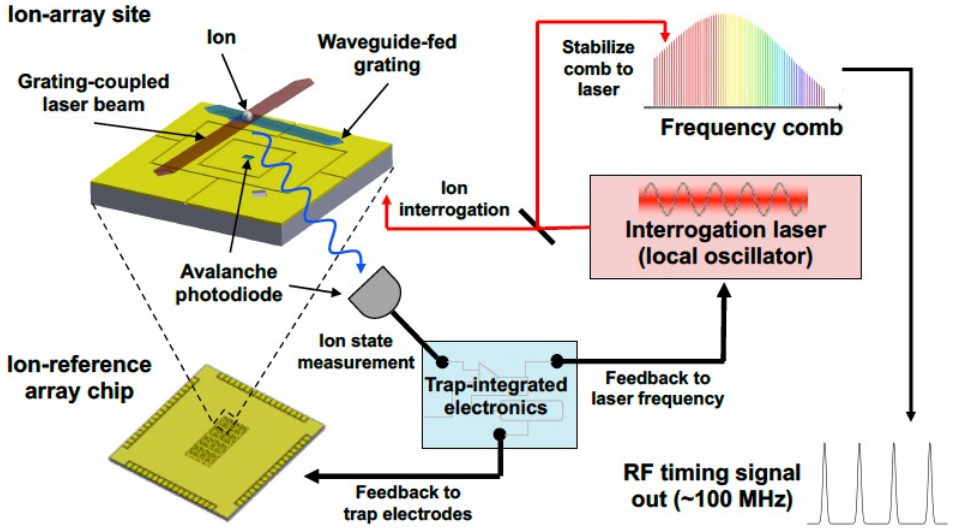
Atomic Clock: Joint DOD – DOE project

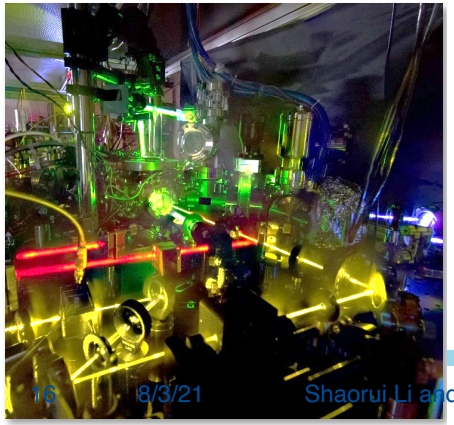
H. Sun, S. Li (FNAL)
J. Chiaverini, R. McConnell (MIT LL)

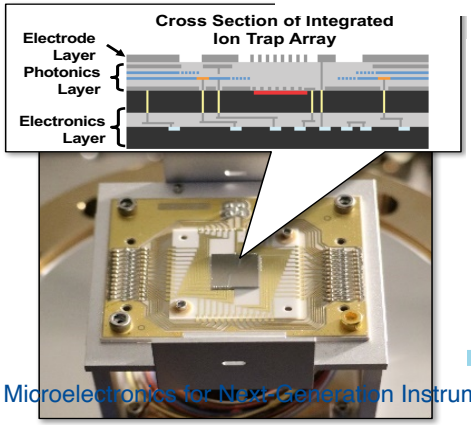
Portable optical atomic clock with frequency instability of 10^{-16} over 10,000 sec

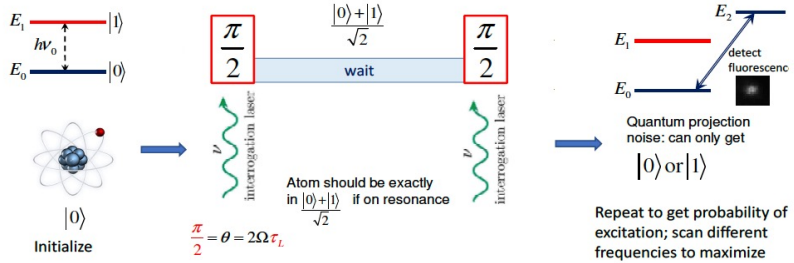
DOD – Atomic Photonic Integration
DOE – Electronic Photonic Integration

Create a closed loop compact system









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Hardware-Software Codesign: AI

Why do we need data processing on the edge

POWER: CV^2f x (data volume) problem

- Total power consumption to move data from pixel to periphery: 1 pJ/bit (~5 mm distance)
- Total power consumption to move data off-chip: > 0.1 nJ/bit

Minimize C,V

- 3D Integration (high density, low capacitance interconnect)
- Low voltage signaling

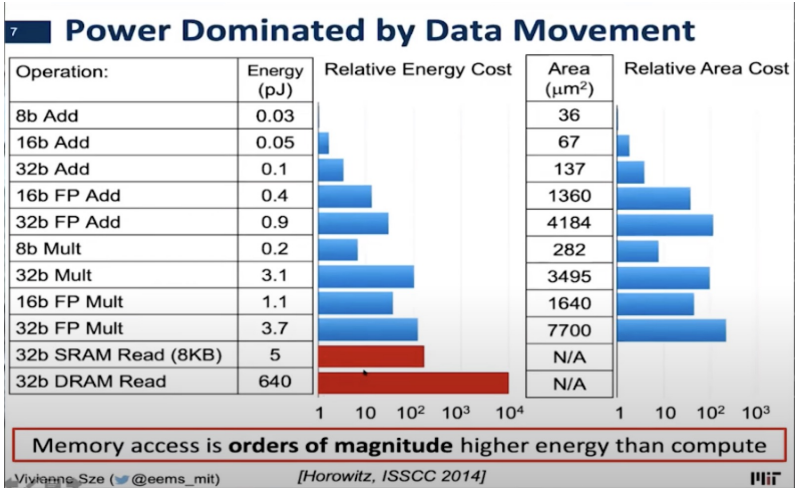
Reduce data

- Typically, just zero-suppression for on-detector sparce data

HL LHC:

Higher granularity, higher occupancy, higher precision

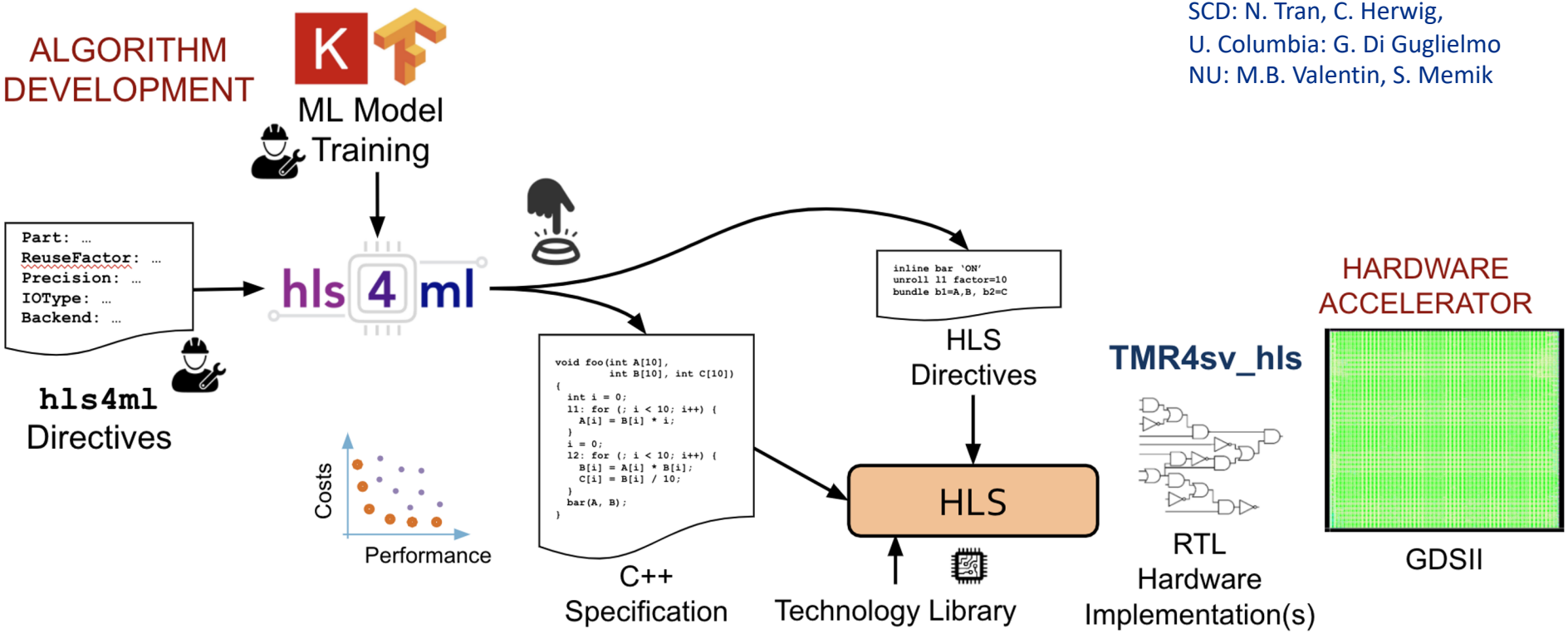
=> needs NEW APPROACH



Tool-kit development and Operation in rad-hard environment

- Integration of HLS generated and expert RTL
- Design code agnostic approach for implementation of various triplication methods

SCD: N. Tran, C. Herwig,
U. Columbia: G. Di Guglielmo
NU: M.B. Valentin, S. Memik

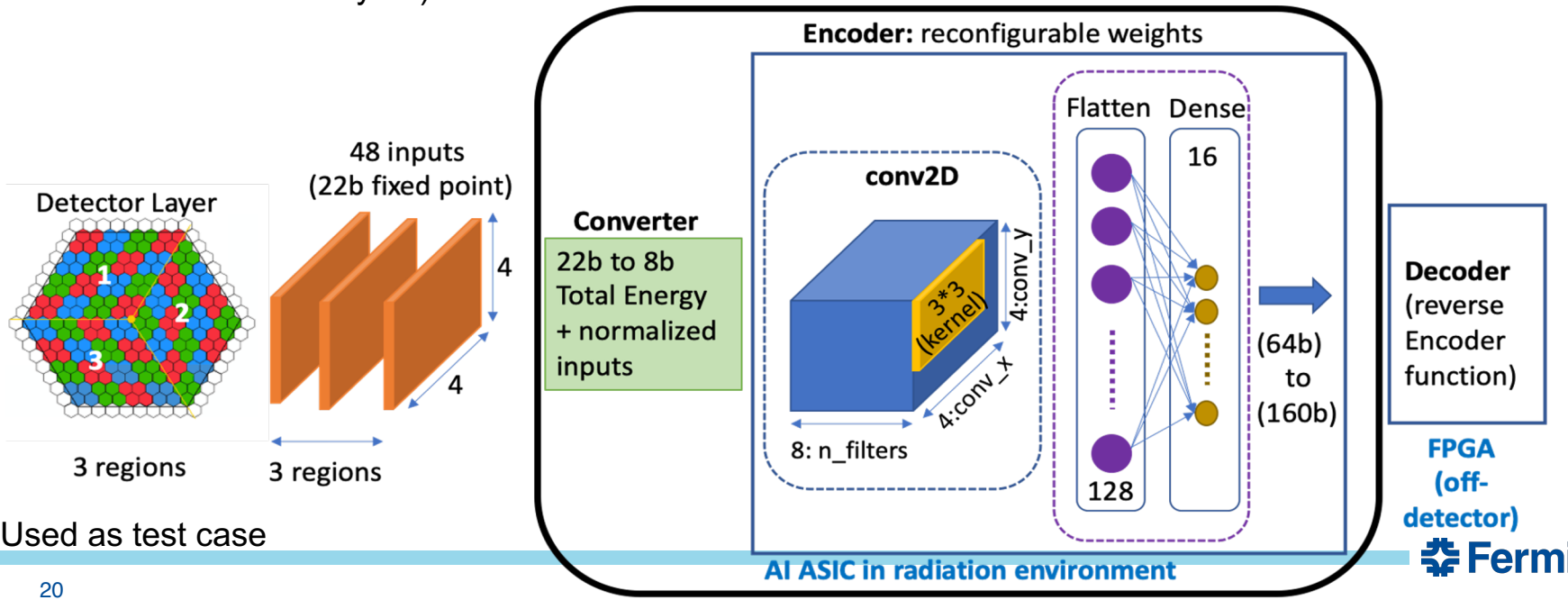


HL LHC High Granularity Calorimeter*: Data flow

J. Hirschauer
SCD: N. Tran, C. Herwig,
U. Columbia: G. Di Guglielmo
NU: M.B. Valentin, S. Memik

CNN: Encodes information by correlating spatial features

- **conv2D layer** – extract spatially corelated geometric features
- **Flatten layer** – Vectorizes the 2D image from the conv2D layer [8 x 4 x 4 = 128 x 1]
- **Dense layer** – aggregates the various features to provide higher order information
- **ReLU** – an activation function which introduces non-linearity by applying thresholds (part of both the conv2D and dense layers)



*Used as test case

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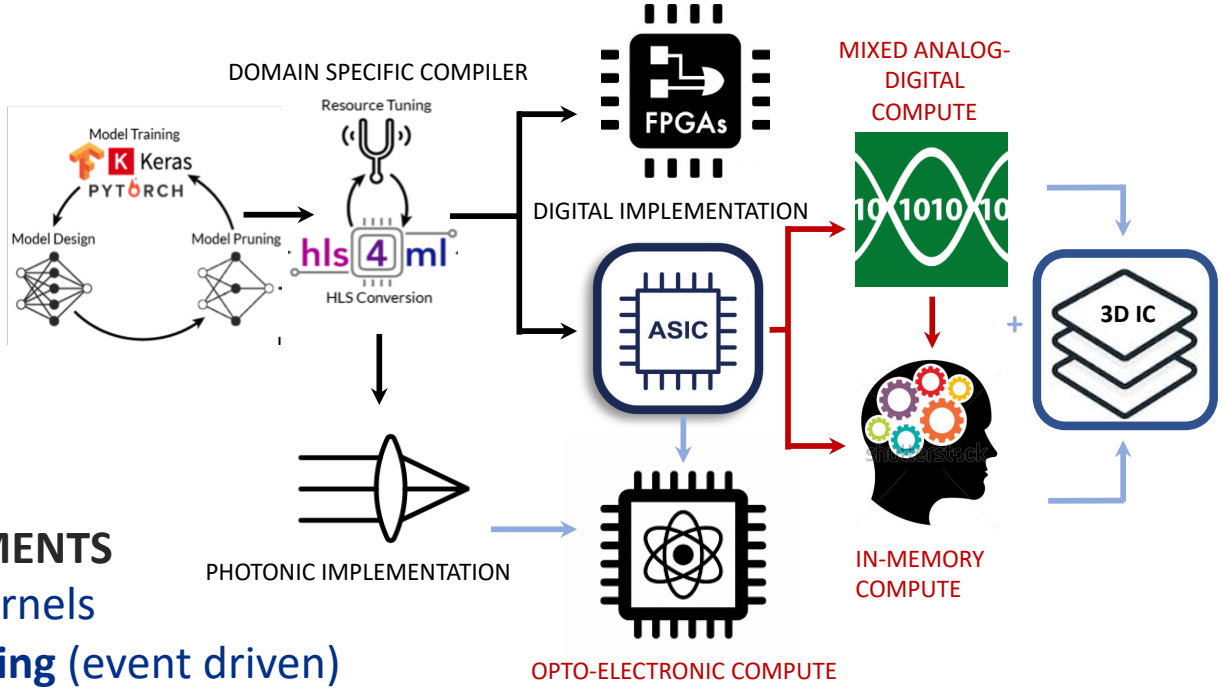
Towards heterogenous system on-chip



OPTIMIZATION REQUIREMENTS

- Analog Mixed-Signal Kernels
- **Neuromorphic computing** (event driven)
- In-memory compute (**non-Von Neumann approaches**) – new materials
- **Electronic-Photonic conversion**
- **Hybrid integration**

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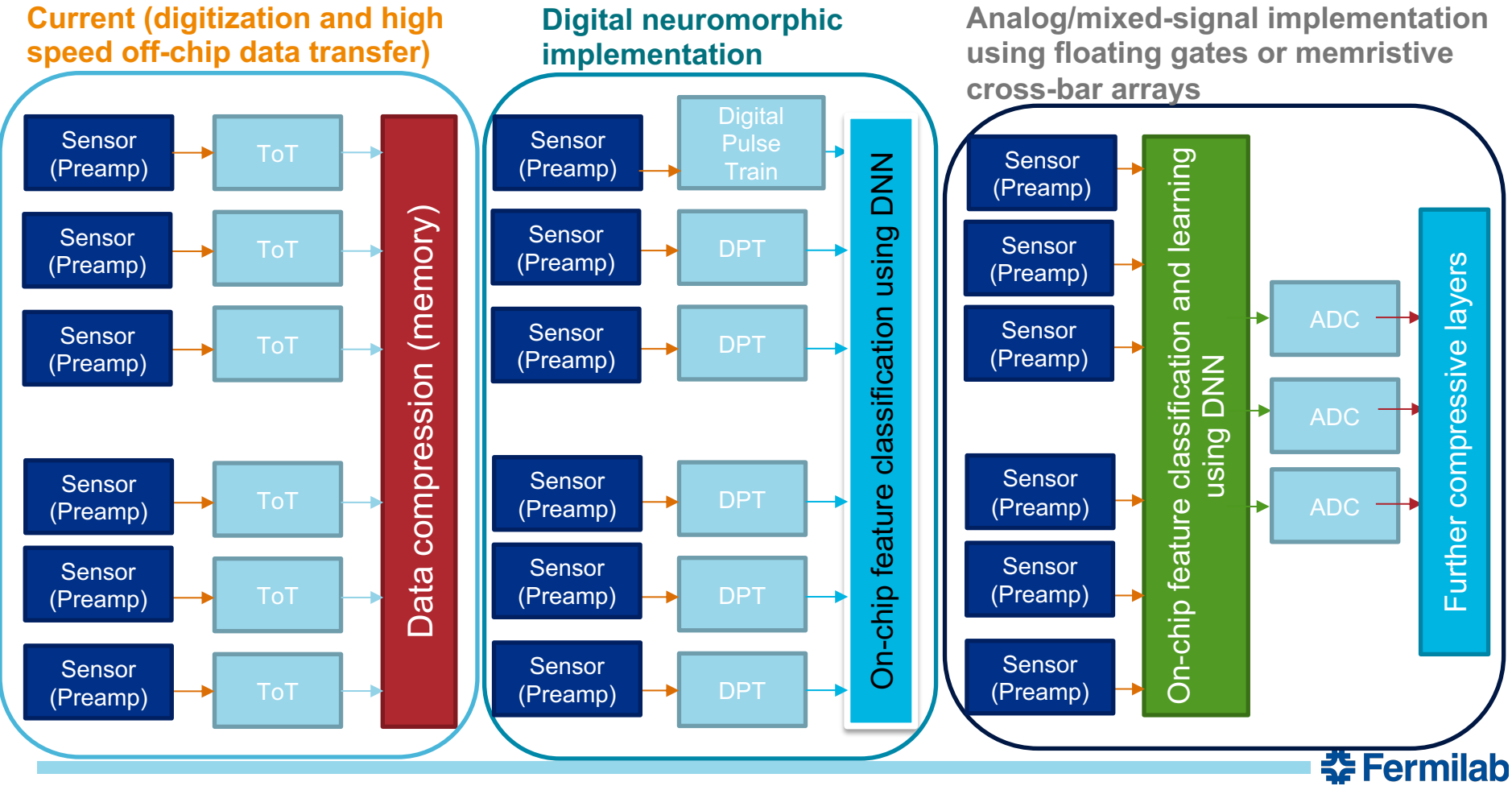
Current (digitization and high speed off-chip data transfer)
Sensor (Preamp)
Sensor (Preamp)
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ToT
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Data compression (memory)
Digital neuromorphic implementation
Sensor (Preamp)
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Digital Pulse Train
DPT
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On-chip feature classification using DNN
Analog/mixed-signal implementation using floating gates or memristive cross-bar arrays
Sensor (Preamp)
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On-chip feature classification and learning using DNN
ADC
ADC
ADC
Further compressive layers

Thank You